IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device, comprising:

a semiconductor layer which includes a first semiconductor region of a first conductivity type, a base region of a second conductivity type, and a plurality of second semiconductor regions of the first conductivity type;

a gate wiring which is formed on the semiconductor layer via a first insulating film;

a plurality of main electrodes which are electrically connected to the plurality of second semiconductor regions and which are insulated from the gate wiring, wherein the gate wiring is arranged between the main electrodes ~~and upper surfaces of the main electrodes are higher than the highest portion of an upper surface of the gate wiring~~; and

a connecting plate which is directly connected onto ~~the~~ upper surfaces of the main electrodes, wherein the main electrodes are in contact with a contact region of the connecting plate, and, in an area under the contact region of the connecting plate, the upper surfaces of the main electrodes are higher than the highest portion of an upper surface of the gate wiring.

Claim 2 (Withdrawn): The semiconductor device according to claim 1, wherein the uppermost layers of the plurality of main electrodes are a metal layer common to the plurality of main electrodes.

Claim 3 (Withdrawn): The semiconductor device according to claim 2, further comprising a second insulating film which is formed on the surface of the uppermost layer of the gate wiring.

Claim 4 (Original): The semiconductor device according to claim 1, wherein the main electrodes are formed of a plurality of metal layers, and a second insulating film extends between the plurality of metal layers.

Claim 5 (Original): The semiconductor device according to claim 1, wherein the plurality of main electrodes are formed apart from the gate wiring with a gap therebetween.

Claim 6 (Currently Amended): A semiconductor device, comprising:

a semiconductor layer which includes a first semiconductor region of a first conductivity type, a base region of a second conductivity type, and a cell forming region;

at least one main electrode which is electrically connected to a second semiconductor region of the first conductivity type in the cell forming region and which is formed in the cell forming region on the semiconductor layer;

a first gate electrode which is formed in the cell forming region and controls continuity between the first semiconductor region and the second semiconductor region;

a gate wiring which is formed on the semiconductor layer via a first insulating film and which leads out the first gate electrode to an outer peripheral region of the cell forming region~~, wherein an upper surface of the main electrode is higher than the highest portion of an upper surface of the gate wiring~~; and

a first connecting plate which is directly connected onto ~~the~~ an upper surface of the main electrode, wherein the main electrode is in contact with a contact region of the first connecting plate, and, in an area under the contact region of the first connecting plate, the upper surface of the main electrode is higher than the highest portion of an upper surface of the gate wiring.

Claim 7 (Withdrawn): The semiconductor device according to claim 6, wherein the uppermost layers of the plurality of main electrodes are a metal layer common to the plurality of main electrodes.

Claim 8 (Withdrawn): The semiconductor device according to claim 7, further comprising a second insulating film which is formed on the surface of the uppermost layer of the gate wiring.

Claim 9 (Withdrawn): The semiconductor device according to claim 8,

wherein the plurality of main electrodes comprise a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, and

wherein the second main electrode layer is formed on the second insulating film.

Claim 10 (Withdrawn): The semiconductor device according to claim 6, wherein the gate wiring extends to the outer peripheral region of the cell forming region, and

the semiconductor device further comprises a second gate electrode which is formed on the gate wiring extending to the outer peripheral region of the cell forming region.

Claim 11 (Withdrawn): The semiconductor device according to claim 10, wherein the second gate electrode extends to the cell forming region.

Claim 12 (Withdrawn): The semiconductor device according to claim 11, further comprising a third insulating film which is formed on the surface of the gate wiring extending to the outer peripheral region,

wherein the third insulating film extends to the cell forming region, and the second gate electrode is formed on the third insulating film in the cell forming region.

Claim 13 (Withdrawn): The semiconductor device according to claim 12, wherein the main electrode comprises a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, and

the third insulating film extends onto the first main electrode layer.

Claim 14 (Withdrawn): The semiconductor device according to claim 10, wherein the second gate electrode is formed of the same material as the uppermost layer of the main electrode.

Claim 15 (Withdrawn): The semiconductor device according to claim 10, wherein the outer peripheral region of the cell forming region is formed at the outer periphery of a semiconductor chip.

Claim 16 (Withdrawn): The semiconductor device according to claim 15, wherein the second gate electrode is formed at the corner of the outer periphery of the semiconductor chip.

Claim 17 (Withdrawn): The semiconductor device according to claim 6, wherein the plurality of main electrodes are formed apart from the gate wiring with a gap therebetween.

Claim 18 (Withdrawn): The semiconductor device according to claim 10, further comprising a second connecting plate which is directly connected to an upper surface of the second gate electrode, wherein a lead frame is connected to the second connecting plate.

Claim 19 (Withdrawn): The semiconductor device according to claim 6, wherein the gate wiring comprises a first metal layer which is formed on the semiconductor layer and a second metal layer which is formed on the first metal layer.

Claim 20 (Withdrawn): The semiconductor device according to claim 19, wherein the second metal layer contains aluminum (Al).

Claim 21 (Previously Presented): The semiconductor device according to claim 6, wherein the upper surface of the main electrode and the first connecting plate contain aluminum (Al).

Claim 22 (Original): The semiconductor device according to claim 6, wherein the first connecting plate is connected to a lead frame.

Claim 23 (Previously Presented): The semiconductor device according to claim 6, wherein the first connecting plate is connected to the main electrode by ultrasonic bonding.

Claim 24 (Currently Amended): A semiconductor device, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type which is formed on the first semiconductor layer;

a first semiconductor region of the first conductivity type which is formed in a first cell forming region in the second semiconductor layer;

a second semiconductor region of the first conductivity type which is formed in a second cell forming region in the second semiconductor layer;

a first gate electrode which is formed in the first cell forming region and controls continuity between the first semiconductor region and the first semiconductor layer;

a second gate electrode which is formed in the second cell forming region and controls continuity between the second semiconductor region and the first semiconductor layer;

a first main electrode which is electrically connected to the first semiconductor region and formed in the first cell forming region on the second semiconductor layer;

a second main electrode which is electrically connected to the second semiconductor region and formed in the second cell forming region on the second semiconductor layer;

a gate wiring which is formed on the second semiconductor layer between the first main electrode and the second main electrode via a first insulating film and which leads out the first and second gate electrodes to an outer peripheral region of the first and second cell forming regions~~, wherein an upper surface of the first main electrode and an upper surface of the second main electrode are higher than the highest portion of an upper surface of the gate wiring~~; and

a first connecting plate which is directly connected onto ~~the~~ upper surfaces of the first main electrode and the second main electrode, wherein the first main electrode and the second main electrode are in contact with a contact region of the first connecting plate, and, in an area under the contact region of the first connecting plate, the upper surface of the first main electrode and the upper surface of the second main electrode are higher than the highest portion of an upper surface of the gate wiring.

Claim 25 (Withdrawn): The semiconductor device according to claim 24, wherein the upper surface of the first main electrode and the upper surface of the second main electrode are part of a common metal layer.

Claim 26 (Withdrawn): The semiconductor device according to claim 25, further comprising a second insulating film which is formed on the upper surface of the gate wiring.

Claim 27 (Withdrawn): The semiconductor device according to claim 26,

wherein the first main electrode comprises a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, and

wherein the second main electrode layer is formed on the second insulating film.

Claim 28 (Withdrawn): The semiconductor device according to claim 25,

wherein the gate wiring extends to the outer peripheral region of the first and second cell forming regions, and

the semiconductor device further comprises a third gate electrode which is formed on the gate wiring extending to the outer peripheral region of the first and second cell forming regions.

Claim 29 (Withdrawn): The semiconductor device according to claim 28, wherein the third gate electrode extends to the first or second cell forming region.

Claim 30 (Withdrawn): The semiconductor device according to claim 29, further comprising a third insulating film which is formed on the surface of the gate wiring extending to the outer peripheral region,

wherein the third insulating film extends to the first or second cell forming region, and the third gate electrode is formed on the third insulating film in the first or second cell forming region.

Claim 31 (Withdrawn): The semiconductor device according to claim 30,

wherein the first main electrode comprises a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, and

wherein the third insulating film extends onto the first main electrode layer.

Claim 32 (Withdrawn): The semiconductor device according to claim 28, wherein the third gate electrode is formed of the same material as the upper surface of the first main electrode.

Claim 33 (Withdrawn): The semiconductor device according to claim 28, wherein the outer peripheral region of the first and the second cell forming region is formed at the outer periphery of a semiconductor chip.

Claim 34 (Withdrawn): The semiconductor device according to claim 33, wherein the third gate electrode is formed at the corner of the outer periphery of the semiconductor chip.

Claim 35 (Withdrawn): The semiconductor device according to claim 25, wherein the first main electrode and the second main electrode are formed apart from the gate wiring with a gap therebetween.

Claim 36 (Withdrawn): The semiconductor device according to claim 28, further comprising a second connecting plate which is directly connected to an upper surface of the third gate electrode, wherein a lead frame is connected to the second connecting plate.

Claim 37 (Withdrawn): The semiconductor device according to claim 24, wherein the gate wiring comprises a first metal layer which is formed on the second semiconductor layer and a second metal layer which is formed on the first metal layer.

Claim 38 (Withdrawn): The semiconductor device according to claim 37, wherein the second metal layer contains aluminum (Al).

Claim 39 (Previously Presented): The semiconductor device according to claim 24, wherein the upper surface of the first main electrode, the upper surface of the second main electrode, and the first connecting plate contain aluminum (Al).

Claim 40 (Original): The semiconductor device according to claim 24, wherein the first connecting plate is connected to a lead frame.

Claim 41 (Original): The semiconductor device according to claim 24, wherein the first connecting plate is connected to the first main electrode and the second main electrode by ultrasonic bonding.

Claim 42 (Cancelled).

Claim 43 (Currently Amended): The semiconductor device according to claim ~~42~~ 6, wherein the at least ~~on~~ one main electrode includes a first main electrode and a second main electrode and the gate wiring is one of gate wiring layers and the gate wiring is the uppermost layer of the gate wiring layers under an area in which the first connecting ~~gate~~ plate is connected to the first main electrode and the second main electrode.

Claim 44 (Previously Presented): The semiconductor device according to claim 6, wherein the gate wiring is formed of aluminum (Al)